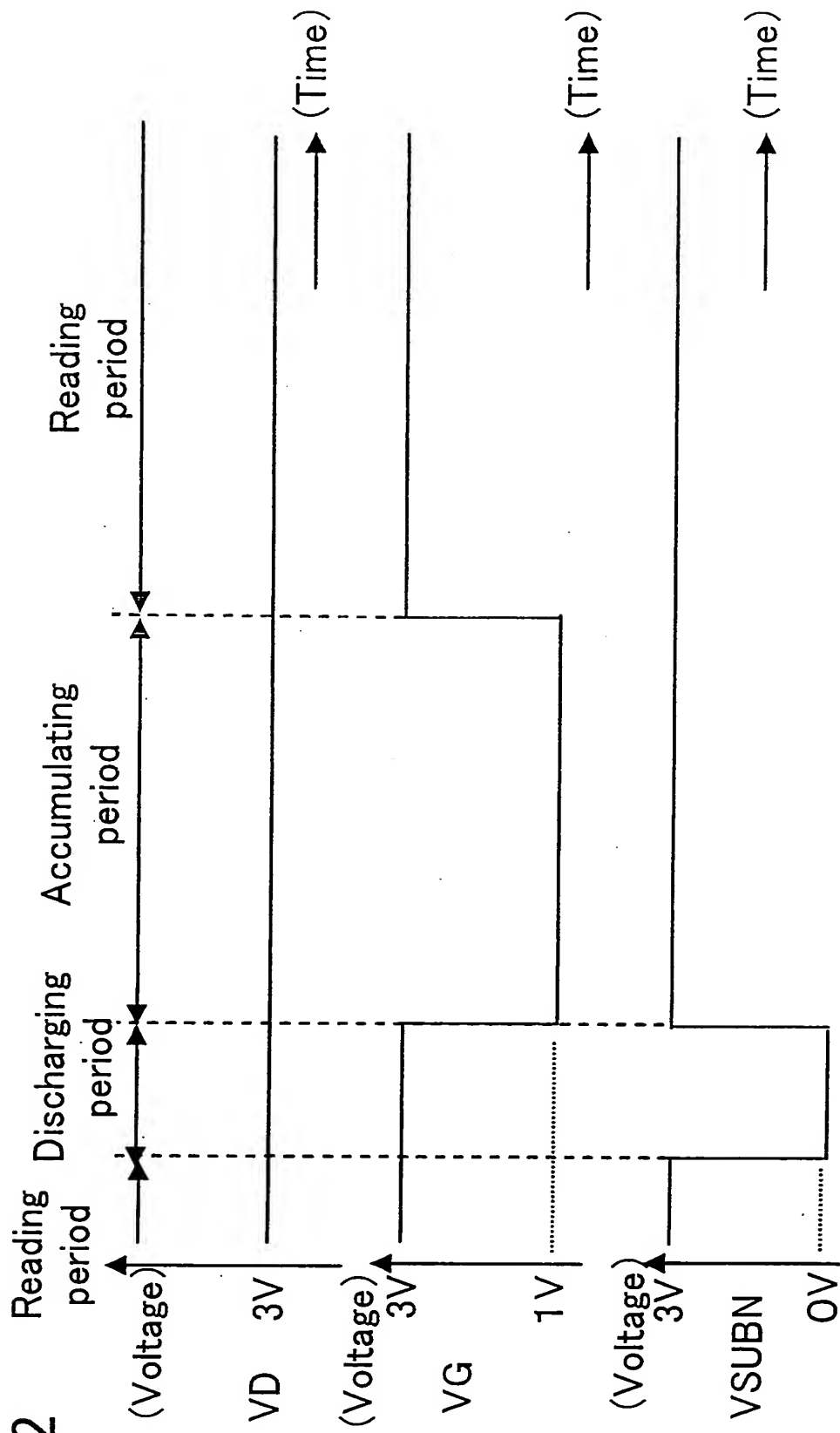


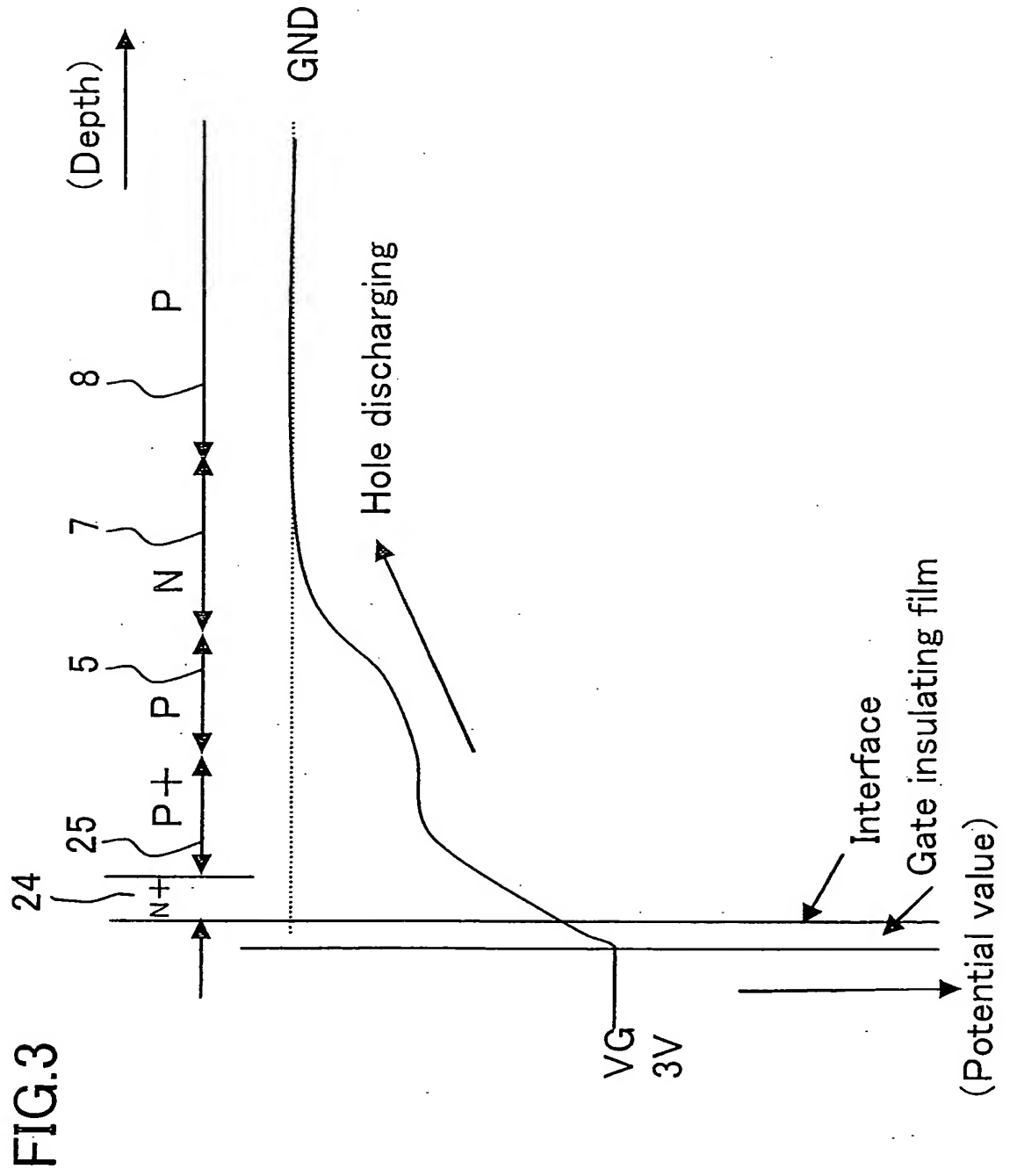
[illegible]

[illegible]

20B

FIG.2





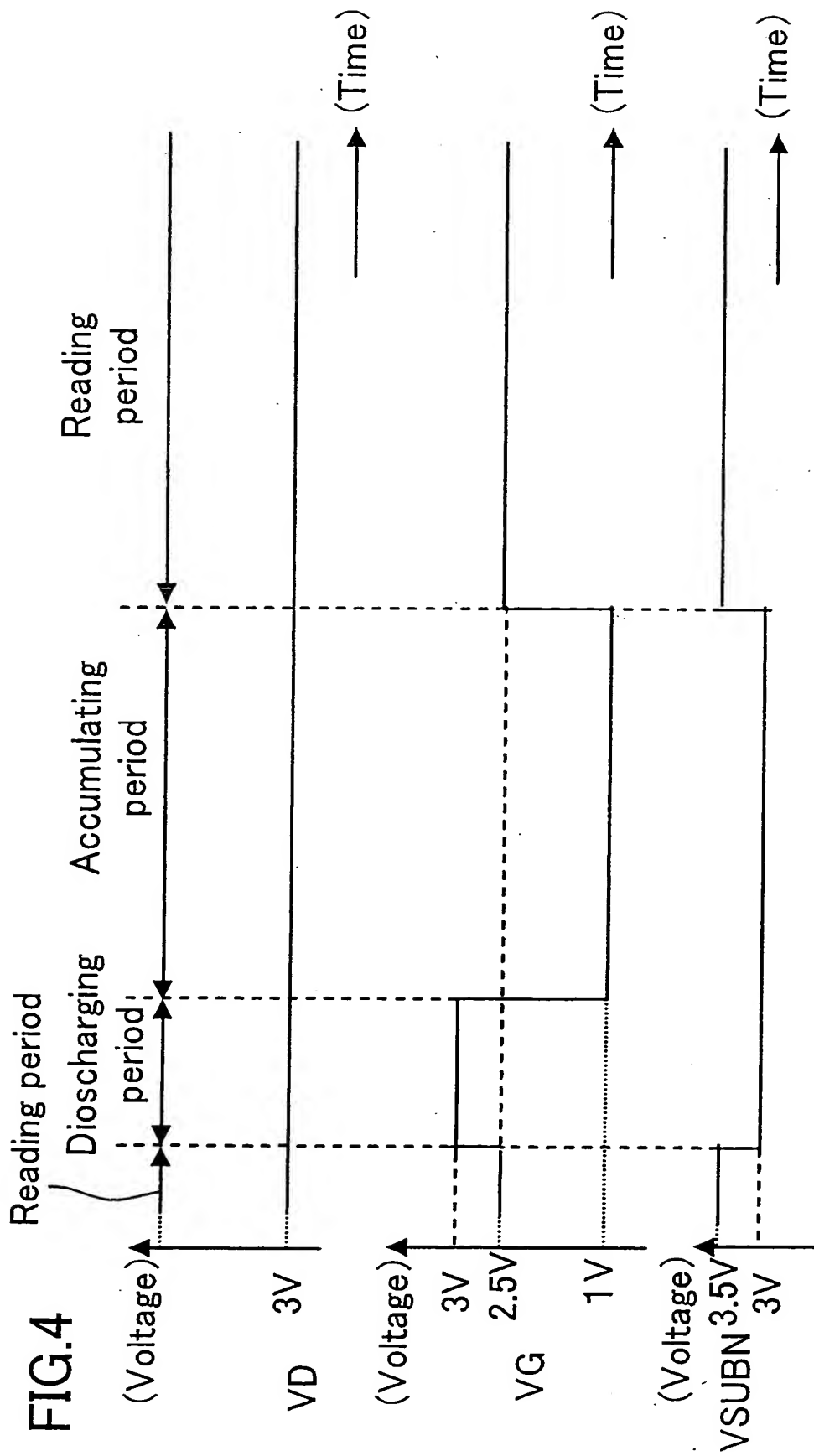


FIG.5

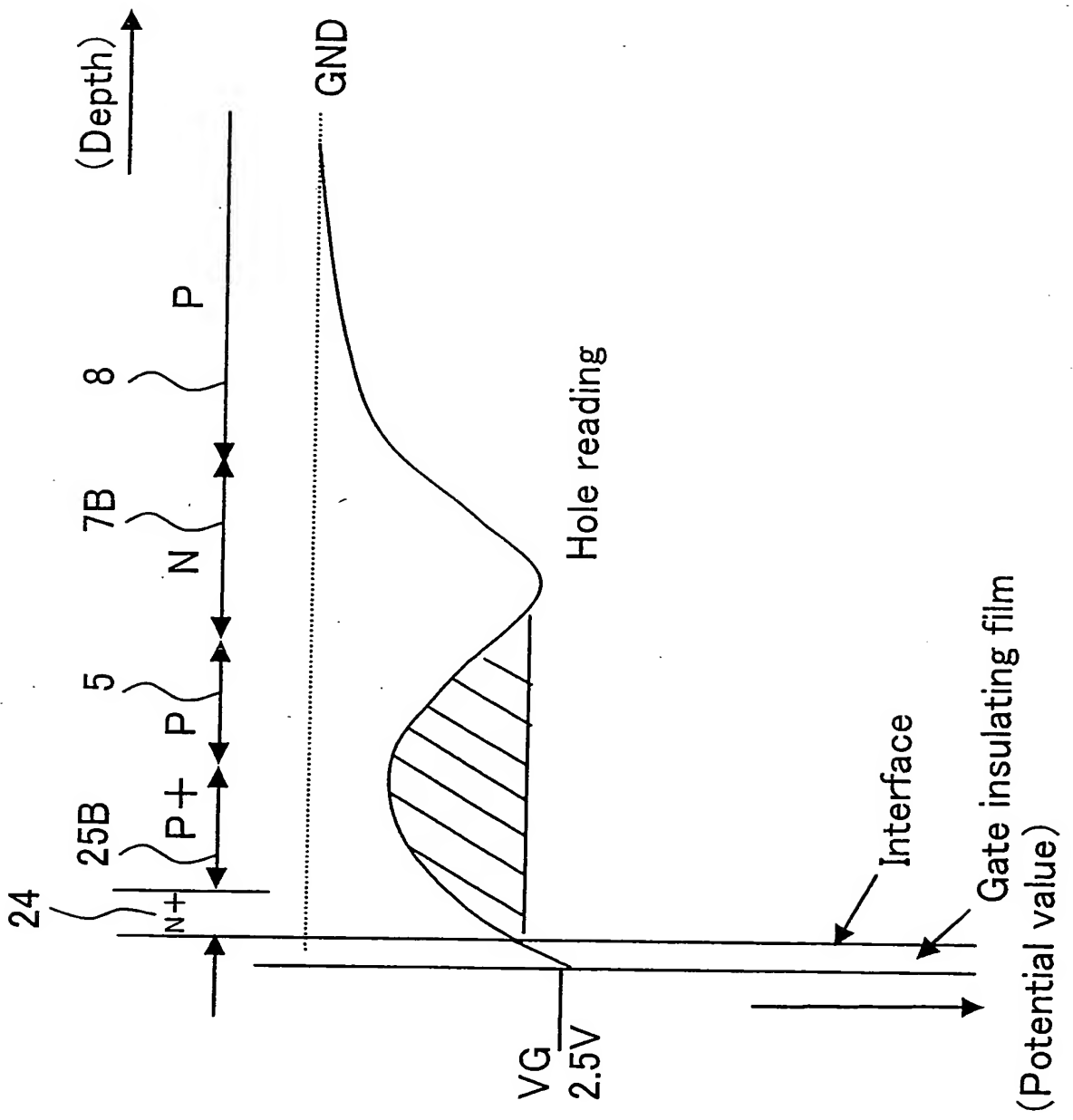
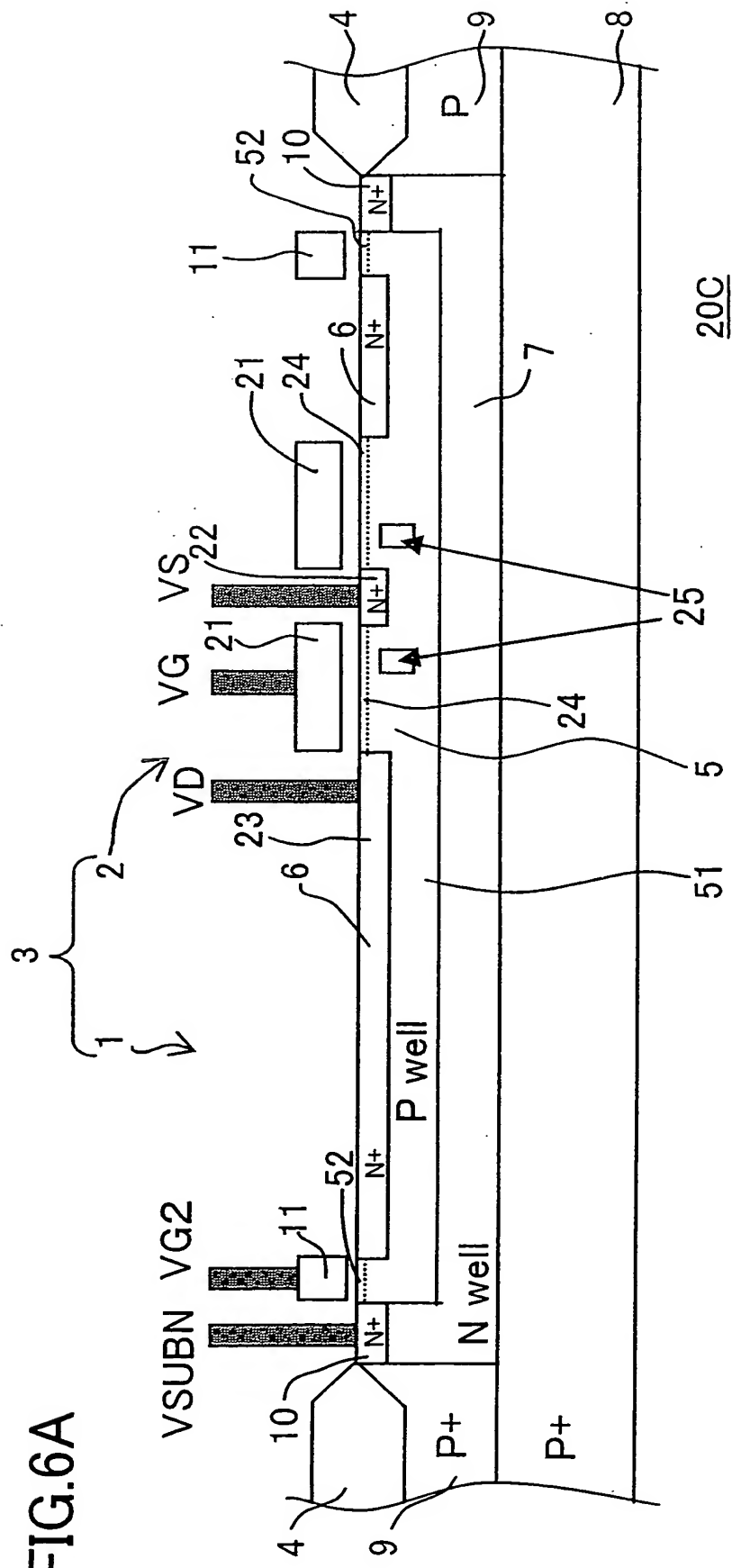


FIG. 6A



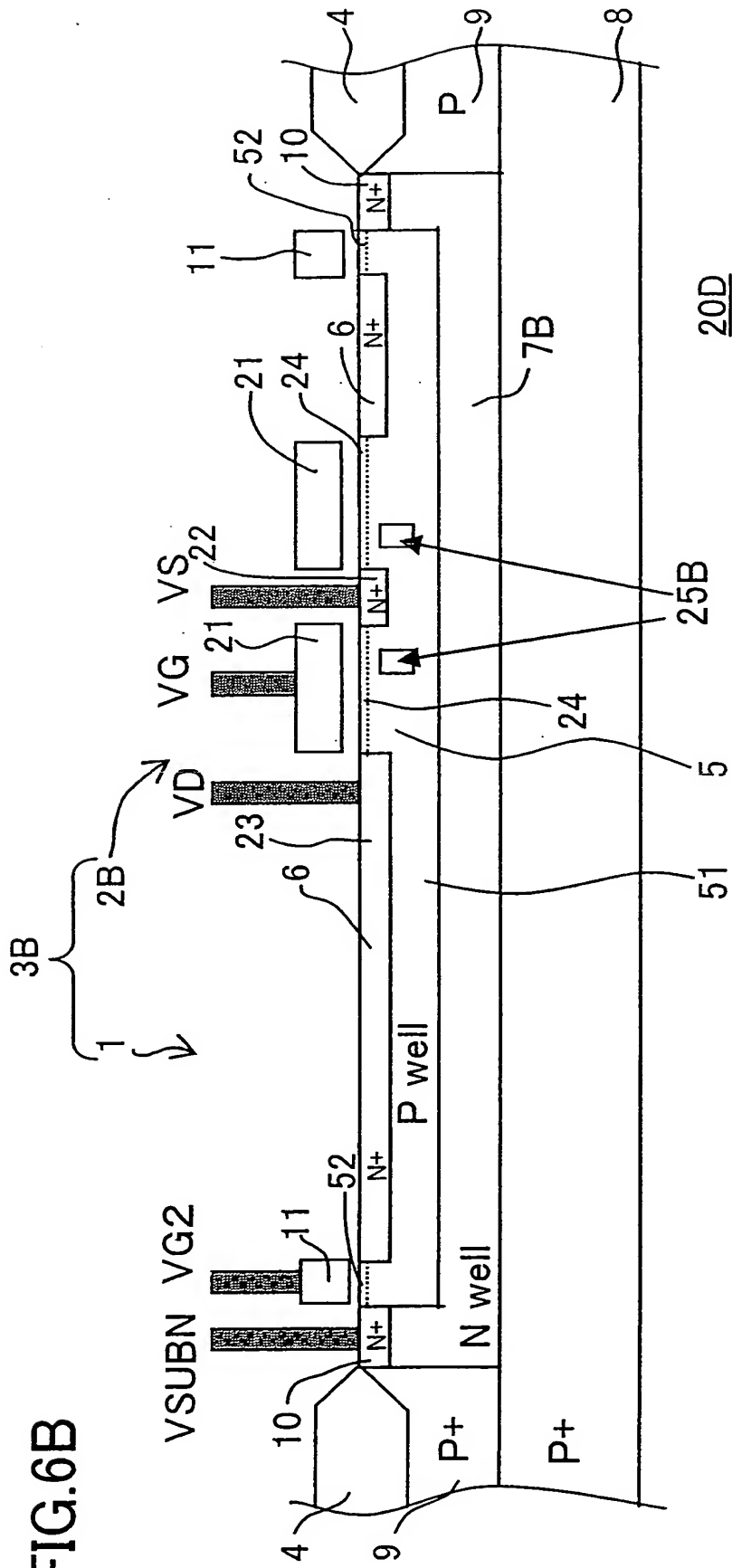
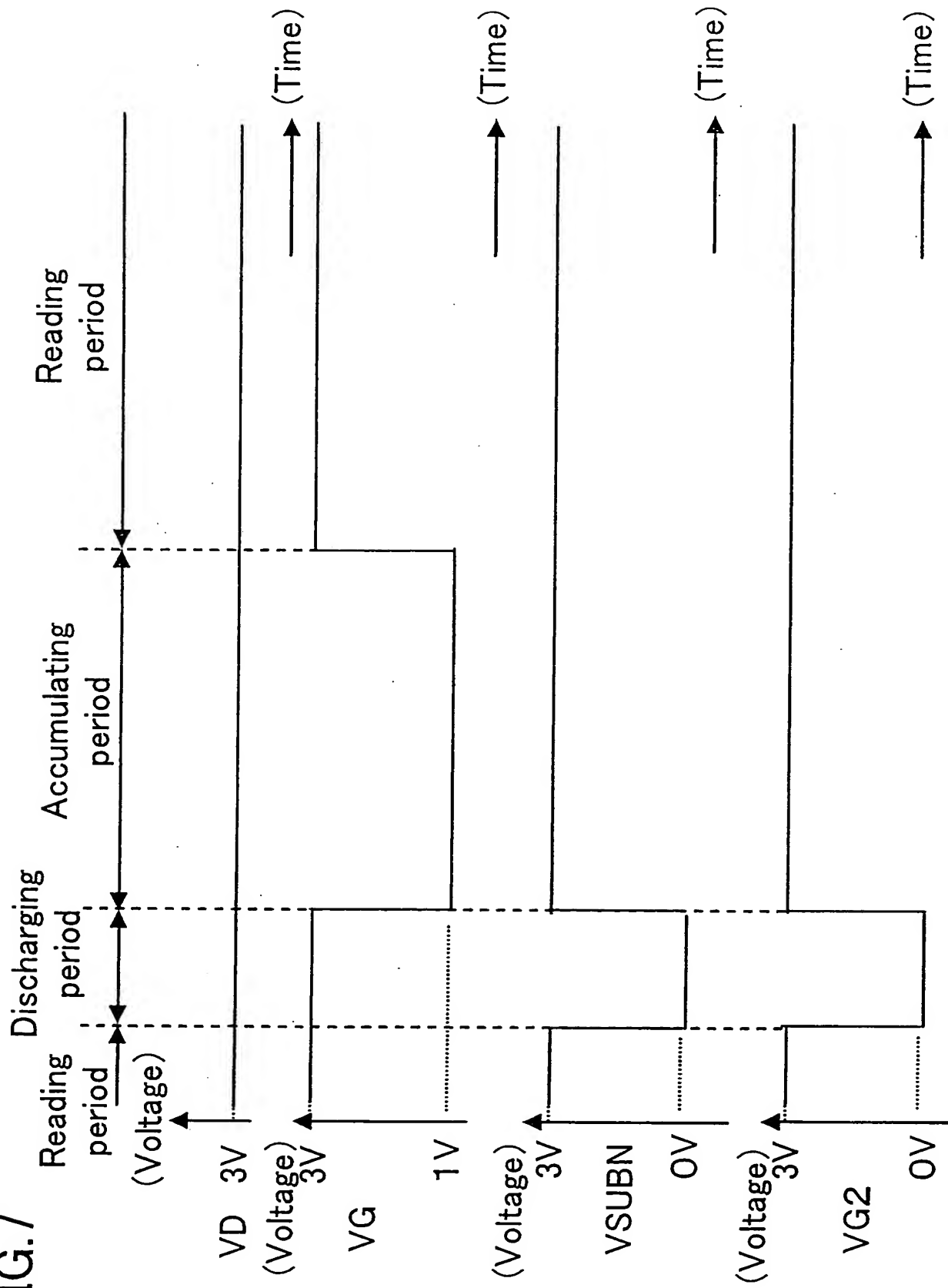


FIG.7



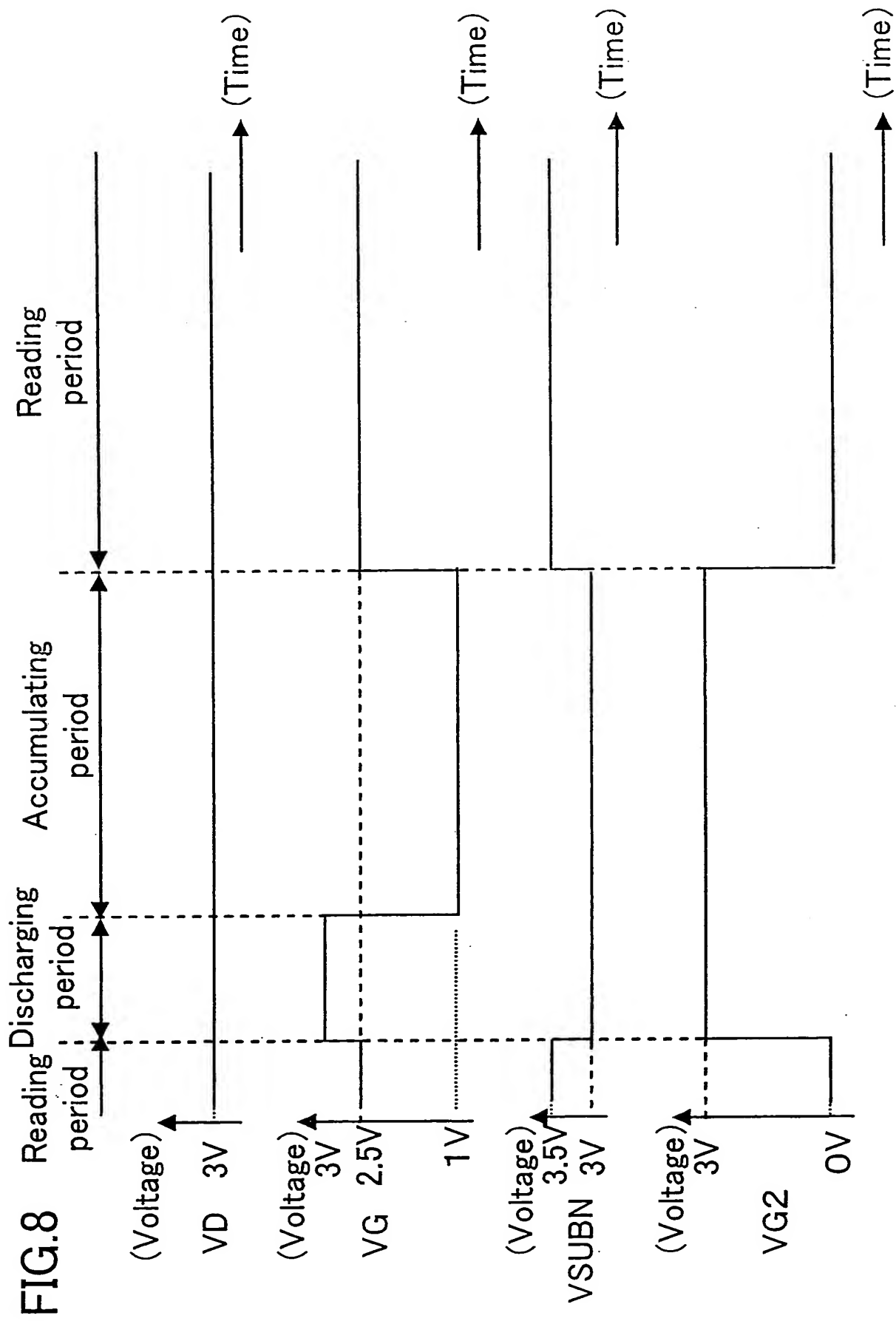


FIG.9

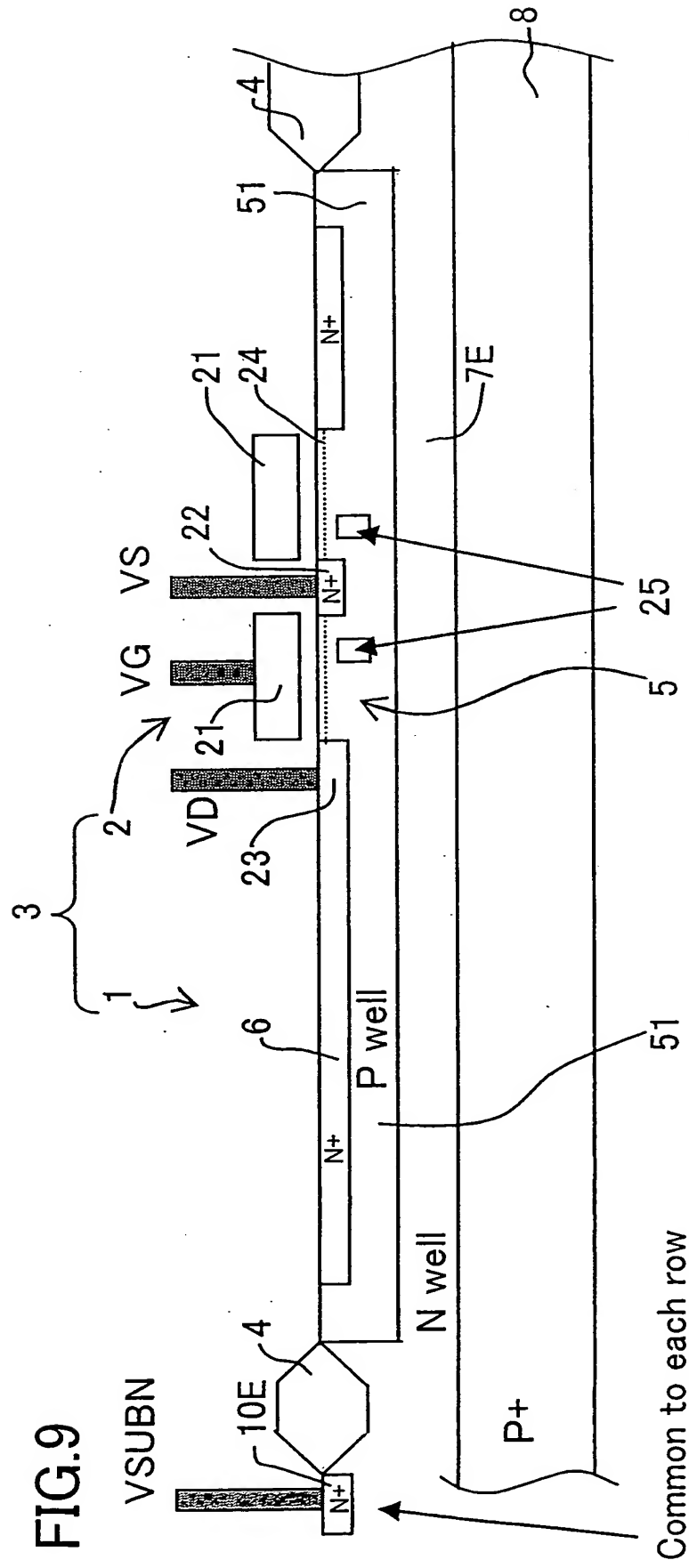


FIG. 10

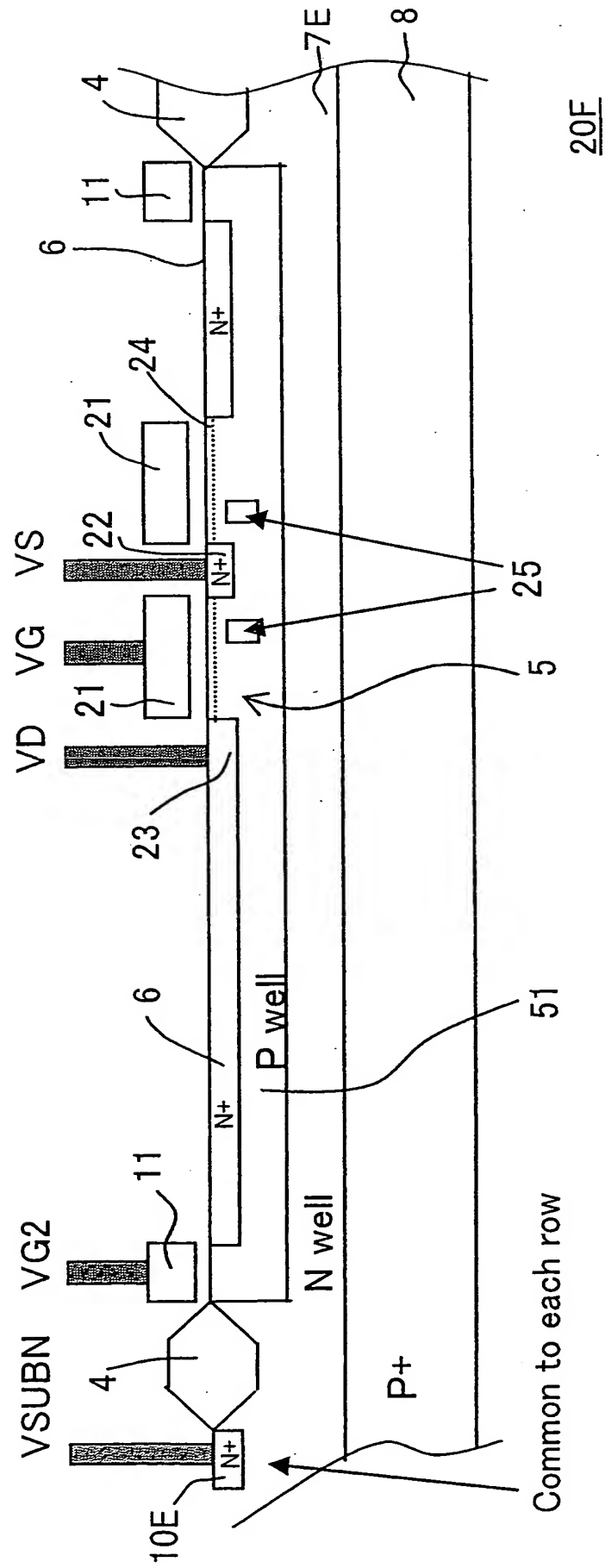


FIG.11

FIG. 11 is a cross-sectional view of a semiconductor device. The device is formed on a substrate (24, 25, 51) which includes P+ regions. A P well is formed in the substrate, and an N well is formed in the P well. The N well contains N+ regions (21, 22, 23). A gate stack is formed on the N+ regions and the P well. The gate stack consists of a gate oxide layer (4), a gate layer (6), and a gate electrode (7H). The gate stack is divided into three sections: 1H, 2H, and 3H. The 1H section is labeled with VD, the 2H section with VG, and the 3H section with VS. The source/drain region is labeled with 20H. The N+ region is labeled with 21, 22, and 23. The P well is labeled with 24, 25, and 51H. The N well is labeled with 24, 25, and 51. The substrate is labeled with 24, 25, and 51.

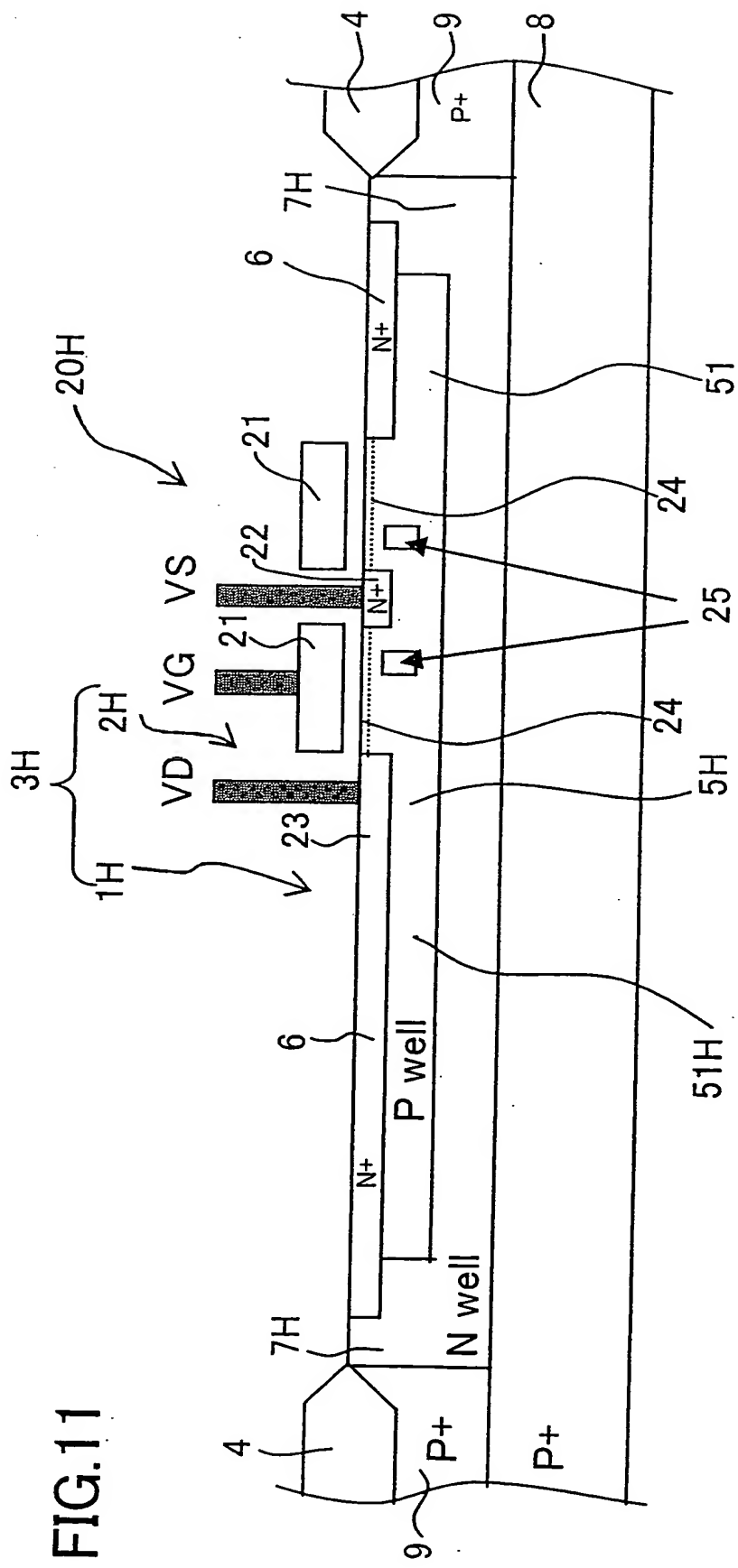


FIG.12

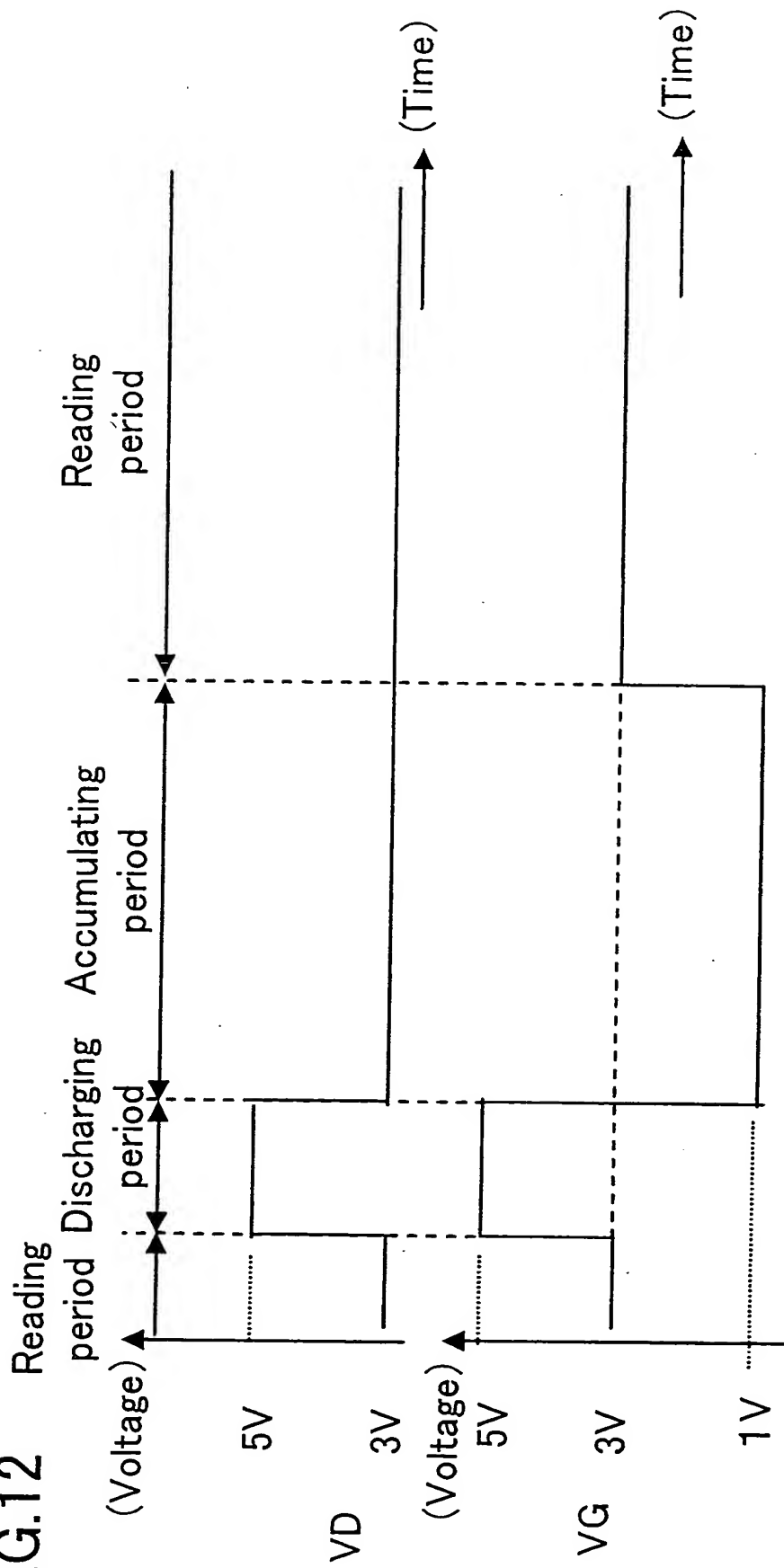


FIG.13

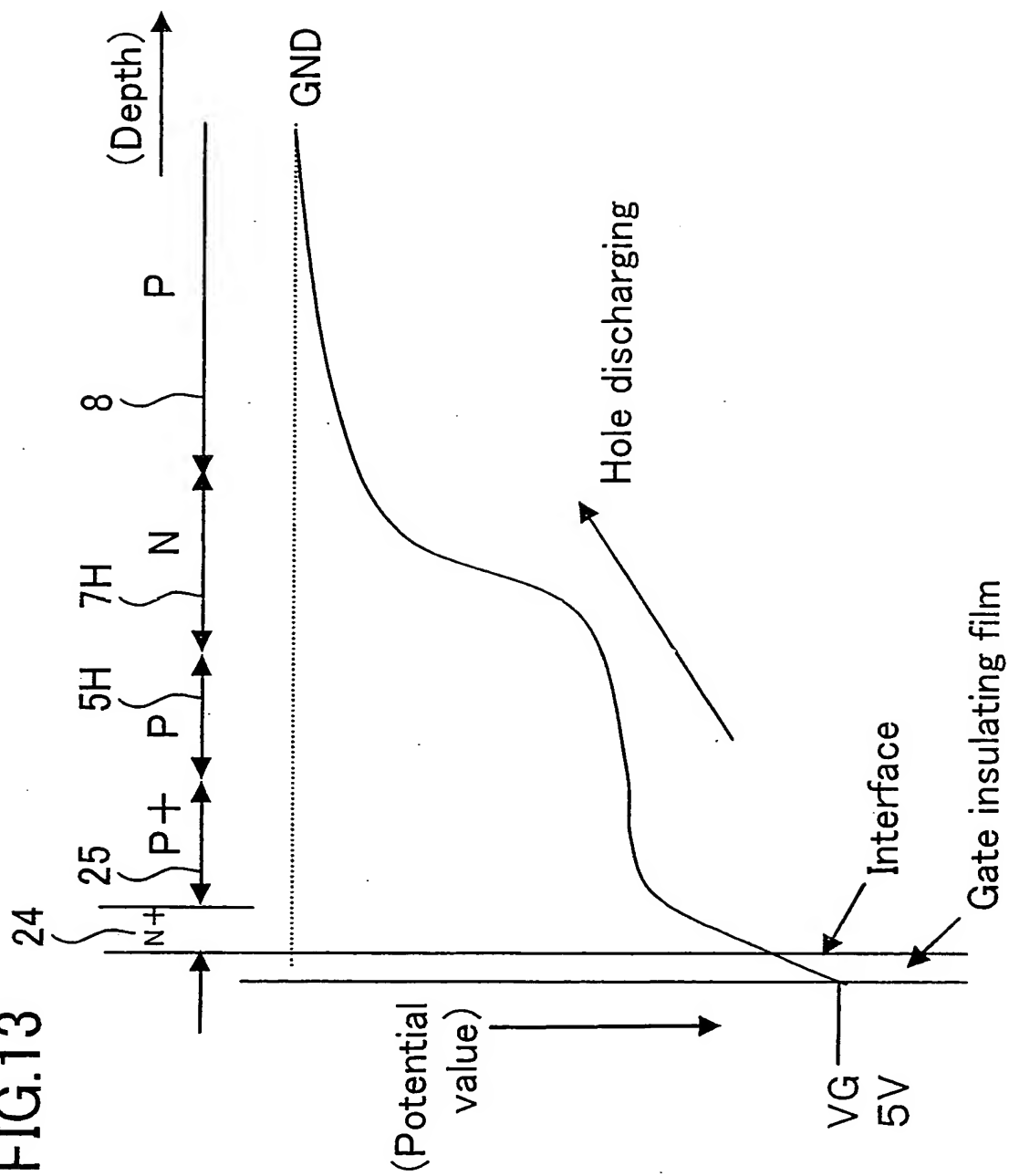


FIG.14

